Reactive Balancing Circuit for Paralleled Battery Modules Employing Dynamic Capacitance Modulation

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Abstract - Battery systems consist of multiple parallel-connected modules to ensure reliability and expand the capacity. However, inconsistency between battery modules causes non-uniform current distribution among branches and results in over-charge or over-discharge issue. To overcome the inconsistency issue, conventional switch-based sequencing or dynamic resistance equalizer regulates the branch current, but it causes increased power losses both in the circuit and inside the battery. This paper proposes a dynamic capacitance modulation scheme that balances the module voltages in the idle mode and regulates the branch currents during the non-idle mode in an efficient way. The operation principle is discussed theoretically and verified by hardware-in-the-loop tests for 4 parallel-connected battery modules. The results show that SOCs are equalized within 1% in the idle mode and the inconsistency is eliminated during the non-idle mode.

Keywords: Dynamic Capacitance Modulation, state of charge (SOC), switched-capacitor (SC) equalizer, parallel-connected battery, SOC equalization.

1. INTRODUCTION

Battery modules are connected in parallel to expand the storage capacity. In the idle mode where there is no energy exchange between battery and external source or load, current flows through parallel branches to stabilize the DC bus voltage. However, the load is distributed to battery branches unequally in the non-idle mode due to the different characteristics of battery cells in capacity, self-discharging rate, impedance, and calendar aging, which is called as cell-inconsistency in parallel connection. It is reported that the unequal current sharing between branches potentially increases the risk of over-charge and over-discharge issue. The investigation in [1, 2] shows that the inconsistency in paralleled modules causes more critical issues than in series configuration.

In a parallel connection of batteries, every open-circuit voltage as well as branch impedance should be identical to distribute the currents evenly. Thus, battery modules are usually binned and screened before the assembling process and only modules with similar characteristics are assembled in direct connection as in Fig. 1(a). However, it requires extra labor and the balancing performance is not always guaranteed due to additional impedance drifts by battery aging. The other conventional method in Fig. 1(b) utilizes sequencing switches per each battery module to adjust the number of modules that are connected to the dc bus [3, 4], but it allows unequal current sharing between branches. Another work in Fig. 1(c) introduces a dynamic resistance equalizer to adjust the branch current [5]. Although it provides an effective way to equalize the SOCs, the power loss in the balancing resistance is its drawback.

In order to solve the inconsistency with reduced power dissipation, this paper proposes a reactive balancing circuit utilizing dynamic capacitance modulation. The topology and working principle are described in section 2, the performance is verified by hardware-in-the-loop (HIL) tests in section 3, and conclusion is made in section 4.

2. PROPOSED EQUALIZER AND OPERATION PRINCIPLES

The proposed equalizer is illustrated in Fig. 2, where it is applied to mSnP configuration such that each battery module consisting of m-series battery cells is connected to a switched-capacitor (SC) cell, and then the outputs of n-SC cells are connected in parallel. The switches are controlled by a complementary PWM signal pair with a variable duty or variable frequency. By applying different gating patterns, the proposed circuit provides two

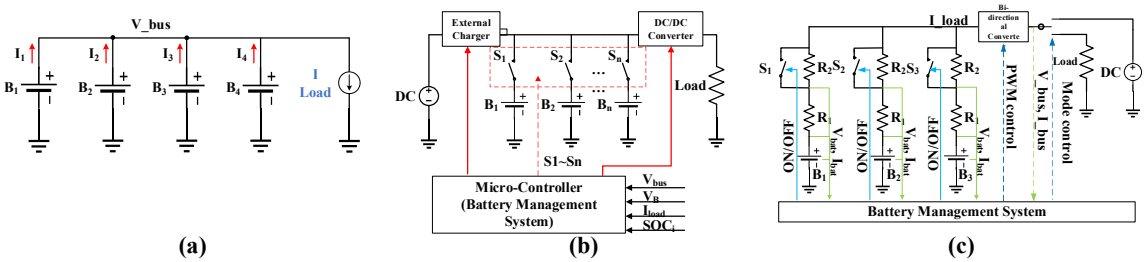

Figure 1: *Conventional methods of paralleling battery: (a) direct connection, (b) switch-based sequencing method, (c) dynamic resistance equalizer.*

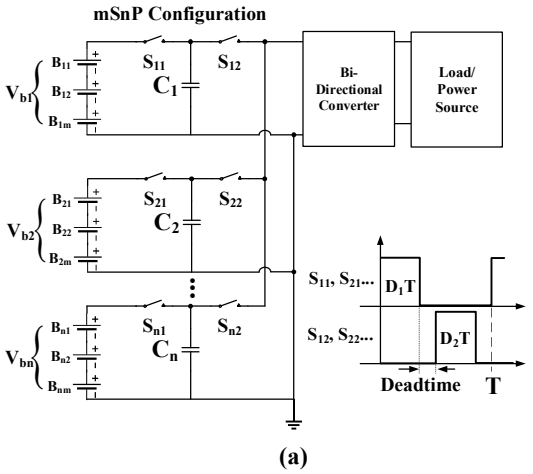

Figure 2: *Topology of the proposed method*

different functions: an autonomous voltage balancing in the idle mode and an active current sharing in the non-idle mode.

2.1. *Variable resistance emulator: Operation analysis*

The SC circuit serves as a variable resistance emulator, which is modeled in Fig. 3(a). When the battery modules are modeled as a voltage source, V_{bk}, and R_{bk} *(k = 1, 2, …, n)* denotes the total sum of ESR of the capacitor and on-resistance of the switches, the SC cell can be regarded as a two-port network, where the voltage between two node *x* and *y* is denoted by ΔV_k in (1).

$$\Delta V_k = V_{bk} - V_{DC\_link} \tag{1}$$

The switches S_1 and S_2 are controlled by a complementary PWM pair as in Fig. 3(b) with two different duty cycles D_1 and D_2 while the pulse period is regarded to be T in this analysis. The operation phase is divided into phases A ($t_0 \sim t_1$) and B ($t_2 \sim t_3$) with a small deadtime interval is inserted between the two phases. In phase A ($t_0 \sim t_1$), the switch S_1 is turned on while S_2 is kept off. By transforming the circuit into the s-domain, we have the equivalent circuit in Fig. 4(a), where v_c is the capacitor voltage. Considering $\tau_1 = R_1 C$ and $\tau_2 = R_2 C$ as the time constants, f_s as the switching frequency, and C as the capacitance, the current through the switches in phase A are calculated by (2) and the energy loss in the resistance R_1 is expressed by (3).

$$i_1(t) = \frac{\Delta V_1}{R_1} e^{\frac{-t}{\tau_1}} = \frac{V_{bk} - v_c(t_0)}{R_1} e^{\frac{-t}{\tau_1}} \tag{2}$$

$$\begin{aligned} E_1 &= \int_{t_0}^{t_1} i_1^2(t) R_1 dt = \int_0^{D_1 T} \left(\frac{\Delta V_1}{R_1}\right)^2 e^{\frac{-2t}{\tau_1}} R_1 dt \\ &= \frac{(\Delta V_1)^2 C}{2} (1 - e^{\frac{-2D_1 T}{\tau_1}}) \end{aligned} \tag{3}$$

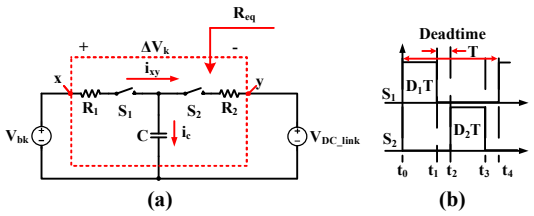

Figure 3: *Operation analysis (a) Model of dynamic capacitance equalizer, (b) complementary PWM control signal.*

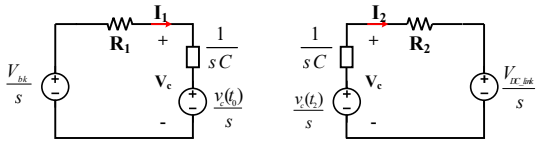

Figure 4: *Equivalent circuit in s-domain: (a) phase A ($t_0 \sim t_1$), (b) phase B ($t_2 \sim t_3$).*

Meanwhile, the in-coming charge to the capacitor during phase A and the capacitor voltage increment is given by (4) and (5), respectively.

$$\begin{aligned} Q_{in} &= \int_{t_0}^{t_1} i_1(t) dt = \int_0^{D_1 T} \frac{\Delta V_1}{R_1} e^{\frac{-t}{\tau_1}} dt \\ &= \Delta V_1 C (1 - e^{\frac{-D_1 T}{\tau_1}}) \end{aligned} \tag{4}$$

$$v_c(t_1) - v_c(t_0) = \frac{Q_{in}}{C} = \Delta V_1 (1 - e^{\frac{-D_1 T}{\tau_1}}) \tag{5}$$

In phase B ($t_2 \sim t_3$), the switch S_1 is turned off while S_2 is turned on and the equivalent circuit in the *s*-domain is illustrated as Fig. 4(b), where the capacitor energy is discharged to the DC link. The current flow through the switch S_2 is calculated by (6). Thus, the energy loss in the resistance R_2 is derived as (7).

$$i_2(t) = \frac{\Delta V_2}{R_2} e^{\frac{-t}{\tau_2}} = \frac{v_c(t_2) - V_{DC\_link}}{R_2} e^{\frac{-t}{\tau_2}} \tag{6}$$

$$\begin{aligned} E_2 &= \int_{t_2}^{t_3} i_2^2(t) R_2 dt = \int_{\frac{T}{2}}^{\frac{T}{2}+D_2 T} \left(\frac{\Delta V_2}{R_2}\right)^2 e^{\frac{-2t}{\tau_2}} R_2 dt \\ &= \frac{(\Delta V_2)^2 C}{2} e^{\frac{-T}{\tau_2}} (1 - e^{\frac{-2D_2 T}{\tau_2}}) \end{aligned} \tag{7}$$

Similarly to phase A, the out-going charge during phase B and the capacitor voltage decrement is calculated by (8) and (9), respectively.

$$\begin{aligned} Q_{out} &= \int_{t_2}^{t_3} i_2(t) dt = \int_{\frac{T}{2}}^{\frac{T}{2}+D_2 T} \frac{\Delta V_2}{R_2} e^{\frac{-t}{\tau_2}} dt \\ &= \Delta V_2 C e^{\frac{-T}{2\tau_2}} (1 - e^{\frac{-D_2 T}{\tau_2}}) \end{aligned} \tag{8}$$

$$v_c(t_2) - v_c(t_3) = \frac{Q_{out}}{C} = \Delta V_2 e^{\frac{-T}{2\tau_2}} (1 - e^{\frac{-D_2 T}{\tau_2}}) \tag{9}$$

With the assumption that the switched capacitor converter is operating in the quasi-steady state condition due to the slow-varying battery voltages, the total charge into the capacitor can be regarded as equal to the charge out of it, $Q_{in} = Q_{out}$, which also means that the capacitor voltage is assumed to be unchanged during the deadtime period: $v_c(t_1) = v_c(t_2)$ and $v_c(t_3) = v_c(t_4)$. Thus, the average capacitor current, I_{c_avg}, is expressed as (10) with $T = 1/f_s$.

$$\begin{aligned} I_{c\_avg} &= Q_{in} f_s = Q_{out} f_s \\ &= \Delta V_1 C f_s (1 - e^{\frac{-D_1}{f_s \tau_1}}) \\ &= \Delta V_2 C f_s e^{\frac{-1}{2 f_s \tau_2}} (1 - e^{\frac{-D_2}{f_s \tau_2}}) \end{aligned} \tag{10}$$

Accordingly, the voltage difference ΔV_1 and ΔV_2 are derived as (11) and (12).

$$\Delta V_1 = \frac{I_{c\_avg}}{f_s C (1 - e^{\frac{-D_1}{f_s \tau_1}})} \tag{11}$$

$$\Delta V_2 = \frac{1}{e^{\frac{-1}{2 f_s \tau_2}}} \frac{I_{c\_avg}}{f_s C (1 - e^{\frac{-D_2}{f_s \tau_2}})} \tag{12}$$

Substituting (11) and (12) into (3) and (7), the energy loss in the series resistance in phases A and B becomes (13) and (14).

$$E_1 = I_{c\_avg}^2 \frac{1}{2 f_s^2 C} \frac{1 + e^{\frac{-D_1}{f_s \tau_1}}}{1 - e^{\frac{-D_1}{f_s \tau_1}}} \tag{13}$$

$$E_2 = I_{c\_avg}^2 \frac{1}{2 f_s^2 C} \frac{1 + e^{\frac{-D_2}{f_s \tau_2}}}{1 - e^{\frac{-D_2}{f_s \tau_2}}} \tag{14}$$

Finally, the total power loss in the circuit is calculated from the total energy loss (E_1+E_2) by multiplying it with the switching frequency, f_s, as in (15).

$$\begin{aligned} P_{loss} &= (E_1 + E_2) f_s \\ &= I_{c\_avg}^2 \frac{1}{f_s C} \frac{\exp(\frac{D_1}{f_s \tau_1}) \exp(\frac{D_2}{f_s \tau_2}) - 1}{\left[\exp(\frac{D_1}{f_s \tau_1}) - 1\right]\left[\exp(\frac{D_2}{f_s \tau_2}) - 1\right]} \end{aligned} \tag{15}$$

On the other hand, by denoting R_{eq} as the equivalent resistance of the SC cell that has seen from the x-y terminal in Fig. 3(a), the power loss in the SC circuit can be expressed by (16).

$$P_{loss} = I_{c\_avg}^2 R_{eq} \tag{16}$$

By equating (15) and (16), the equivalent resistance of the SC circuit, Req, is derived as (17) which is a function of duty ratio (D_1, D_2), capacitance, C, and switching frequency, f_s.

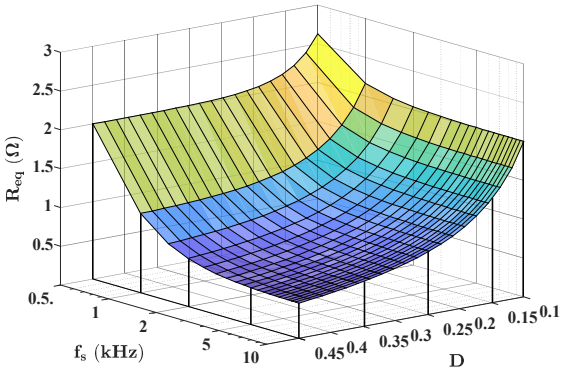

Figure 5: *Equivalent resistance of SC cell R_{eq} as a function of f_s and D (C = 2200uF).*

$$R_{eq} = \frac{1}{f_s C} \frac{\exp(\frac{D_1}{f_s \tau_1}) \exp(\frac{D_2}{f_s \tau_2}) - 1}{\left[\exp(\frac{D_1}{f_s \tau_1}) - 1\right]\left[\exp(\frac{D_2}{f_s \tau_2}) - 1\right]} \tag{17}$$

$$R_{eq} = \frac{1}{f_s C} \frac{1 + \exp(\frac{-D}{f_s \tau})}{1 - \exp(\frac{-D}{f_s \tau})} \tag{18}$$

When it is further assumed that $D_1=D_2=D$ and $\tau_1=\tau_2=\tau$, the equivalent resistance can be further reduced to (18), which also matches with formula in [6]. Fig. 5 illustrates that the equivalent resistance of SC cell can be regulated by changing the switching frequency, f_s, and duty ratio, D, with a specific capacitance, C, and is inversely related to duty ratio, D, and switching frequency, f_s. In this paper, the switching frequency control is adopted to modulate the R_{eq}.

2.2. *Non-idle mode operation: Active current sharing*

The variable-resistance feature of the SC cell can be utilized as a current sharing circuit in the non-idle mode operation of the paralleled battery configuration as in Fig. 6(a). By controlling the SC equalizer with the different switching frequency, the branch currents are regulated. The lower switching frequency or duty ratio, the higher branch resistance is achieved to reduce the branch current.

In discharge mode, based on the measured voltages of battery modules, the SC cell of the lowest voltage module is operated by the minimum switching frequency. On the contrary, in charge mode, the highest voltage module is operated by the minimum switching frequency to increase the equivalent branch impedance and reduce the branch current. Because the role of the lowest/highest voltage module is dynamically changed during the operation process a scanning algorithm, SOCs of modules are gradually equalized by adjusting the switching frequency. Furthermore, if one module is unhealthy, the corresponding SC cell switches are totally turned off to

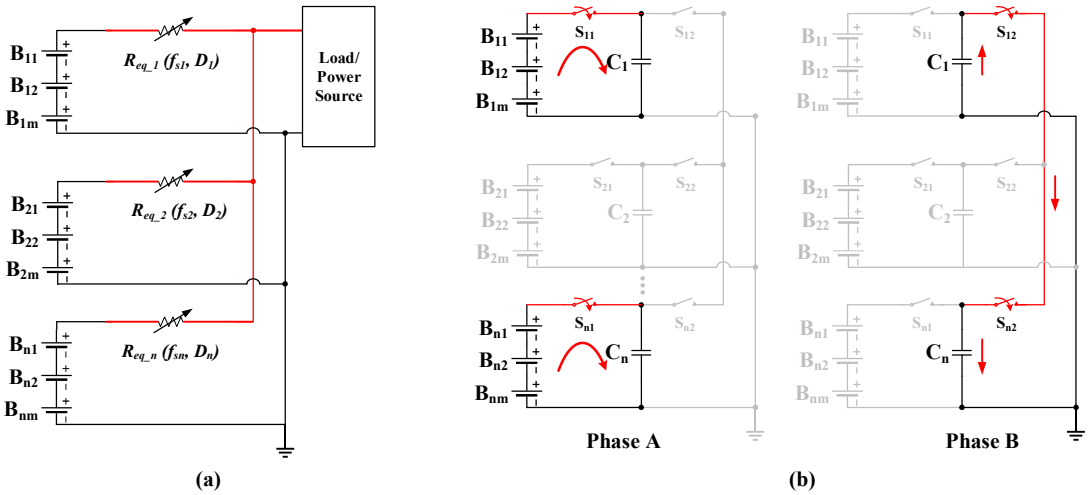

Figure 6: *Operation principle: (a) operations in the non-idle mode, (b) operations in the idle mode.*

isolate the faulty module from the battery bank which is an additional feature of the proposed scheme.

2.3. *Idle mode operation: Autonomous voltage balancing*

In the idle mode where there is no current flow between the battery and load, the proposed circuit works as a SOC balancing circuit that transfers energy from higher voltage module to lower voltage module. Based on the open-circuit voltage of modules, the highest and the lowest voltage modules are detected, and only the switches of those modules are activated by a complementary PWM signal pair as in Fig. 6(b). In this case, the duty ratio is kept as close as 50% and the switching frequency is properly selected to minimize the equivalent resistance, so as to increase the balancing speed. The on-duty is set with a small deadtime to prevent shoot-through. As the charge is transferred directly between two battery modules, the voltages of the modules are gradually equalized. After a few cycles, another highest-lowest voltage module pair is detected and the process repeats. The gate signal will be stopped when every module voltage becomes similar, and the whole module SOC is eventually balanced within a certain level because the battery voltage is closely related to the SOC level.

3. VERIFICATION

3.1. *Experimental setup and performance indices for comparison*

To verify the proposed method, HIL tests are performed for four Li-ion battery modules in the 8S4P configuration, where 8 cells are connected in series as a string and then paralleled in four. The switching frequency of the complementary PWM signal is set to 10kHz with a 45% on duty and 5% deadtime duty for each operation phase. The balancing capacitance is designed to be 2200uF with ESR of 0.1Ω, and the on-resistance of IRF8313 MOSFET is regarded as 21.6 mΩ. In the implementation of the conventional resistive balancing scheme in Fig. 1(c), the equalization resistors, R_1, and R_2, are set to 0.1Ω and 0.5Ω, respectively, which is claimed to be optimal in [5].

In the non-idle mode test, battery modules are discharged by a 4A constant current and charged by a 4A-4.2V CC-CV method, and the switching frequency for the reactive balancing circuit of the highest voltage module (in charging mode) and the lowest voltage module (in discharging mode) is adjusted to 1kHz. The test is stopped when any module becomes fully charged or discharged. While the conventional and the proposed methods are tested during the same operation time and under the same condition, the equalization performance is evaluated by the degree of SOC equalization (DoSE) and the degree of voltage equalization (DoVE) as defined in [5]. Meanwhile, the equalization speed of equalizer is evaluated by the required time for SOC level difference to be less than 1%.

To investigate the impact of the pulsating current waveform, the total power loss is decomposed into the total external loss (in the circuit) and the total internal loss (inside the battery). Based on the HIL test results, the external loss of the conventional resistance equalizer, and the proposed method is calculated by (19). On the contrary, the external loss of the switch-based sequencing method in Fig. 1(b) is expressed by (20).

$$P_{loss\_external} = \sum_{m=1}^{N} \frac{1}{t_3} \int_0^{t_3} i_m^2(t) Z_m(t) dt \qquad (19)$$

$$P_{loss\_external} = \sum_{m=1}^{N} \frac{1}{t_3} \int_0^{t_3} i_m^2(t) R_{d\_on} dt \qquad (20)$$

where $i_m(t)$ is the measured current flowing each branch, $Z_m(t)$ is the branch impedance, which is determined by either R_{eq_high} (when it is not playing the role of the lowest voltage module) or R_{eq_low} (during the role of the

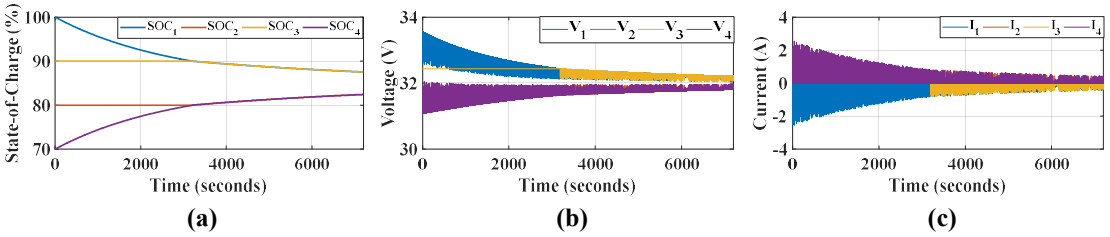

Figure 7: Equalization process in idle mode *(a) SOC profiles, (b) module voltage profiles, (c) branch current profiles.*

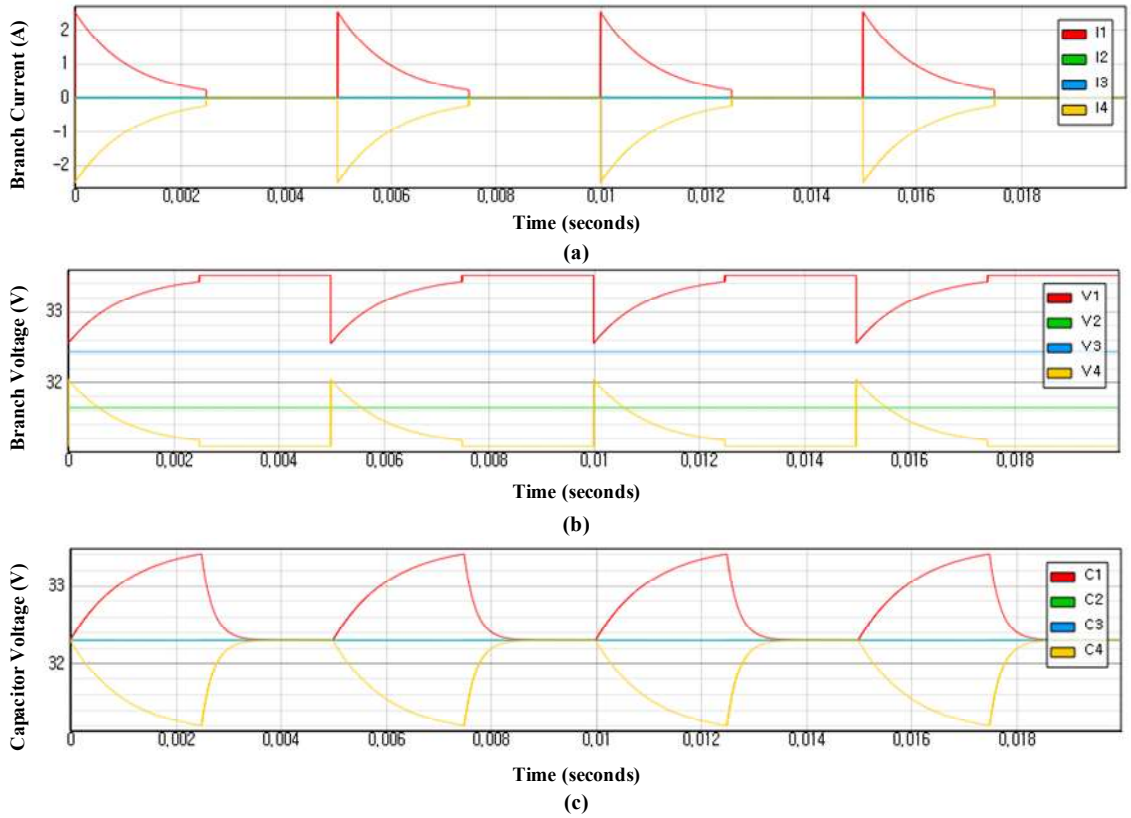

Figure 8: *Operation waveform in the idle mode: (a) branch currents, (b) battery voltages, (c) capacitor voltages.*

lowest voltage module), and R_{d_on} is the on-resistance of MOSFET.

Similarly, the internal power loss of batteries is calculated by (21), where R_b is the total internal DC impedance of battery in series strings, which is provided in the datasheet [7].

$$P_{loss\_internal} = \sum_{m=1}^{N} I_{rms\_m}^2 R_b \qquad (19)$$

3.2. *Test results in the idle mode*

In the idle mode, the initial SOCs of battery modules are set to be different as $SOC_{init1,2,3,4}$ = *100, 80, 90, 70%*. The equalization process is stopped after 7200 seconds and the SOC, voltage, and branch current profiles of the proposed method are illustrated in Fig. 7. The SOC profile in Fig. 7(a) shows that the equalizer requires 3200 seconds to achieve a 10% SOC difference and 7200 seconds to reach a 5% SOC difference as in Fig. 7(a). Besides, the module voltages are equalized within 0.4V as in Fig. 7(b). The equalization speed becomes slower after 3200 seconds due to the small voltage difference between modules. In fact, the SOC of modules can be equalized further but it takes much time due to the small equalization current.

The current profile in Fig. 7(c) and the operation waveform in Fig. 8 represent the equalization strategy of the proposed method. Because only two modules are equalized at the same time, module #1 and #4 takes the role of the highest and the lowest voltage modules in the beginning. When the SOC_1 equals SOC_2 and the SOC_3 equals SOC_4, module #3 and module #2 take over the roles of the highest and the lowest voltage module. As a result, energy is transferred between module #3 and module #2 in the next turn. Likewise, the SOCs of all modules are equalized eventually.

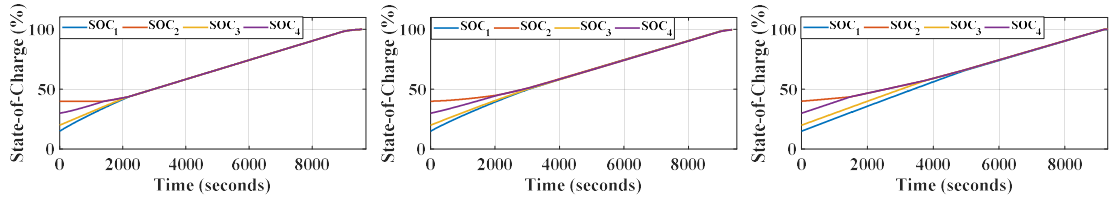

Figure 9: *SOC profile in charging mode (a) switch-based sequencing method, (b) dynamic resistance equalizer, (c) proposed method.*

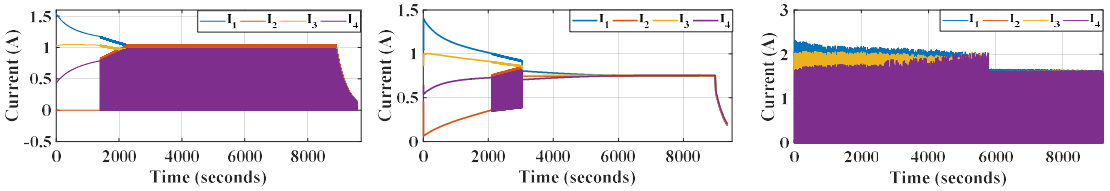

Figure 10: *Branch current profile in charging mode (a) switch-based sequencing method, (b) dynamic resistance equalizer, (c) proposed method.*

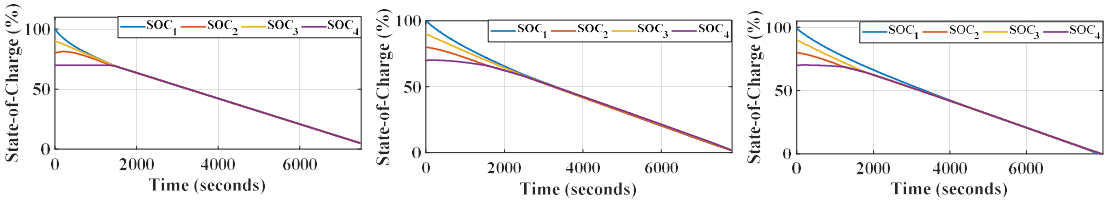

Figure 11: *SOC profile in discharging mode (a) switch-based sequencing method, (b) dynamic resistance equalizer, (c) proposed method.*

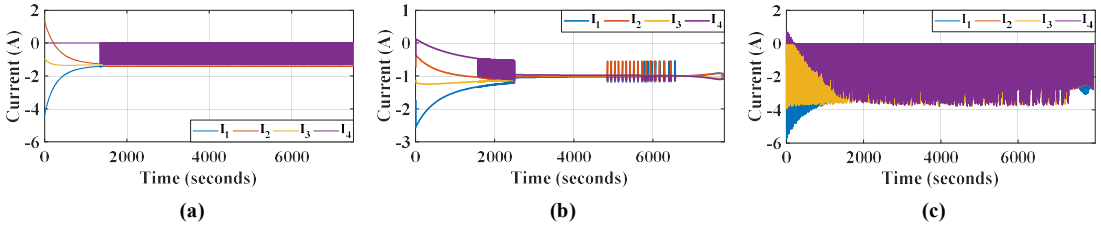

Figure 12: *Branch current profile in discharging mode (a) switch-based sequencing method, (b) dynamic resistance equalizer, (c) proposed method.*

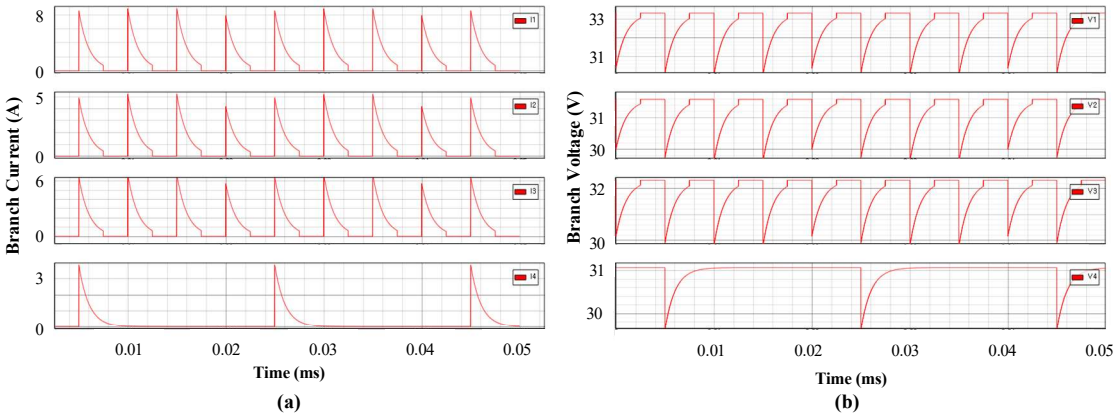

Figure 13: Operation waveform in discharging mode *(a) branch currents, (b) module voltages.*

3.3. *Test results in the non-idle mode*

For the tests in the non-idle mode, the initial SOCs of battery modules are set to be different: $SOC_{init1,2,3,4}$ = 15, 40, 20, 30% during charge mode and $SOC_{init1,2,3,4}$ = 100, 80, 90, 70% during discharge mode. For the three different methods, the SOC and the current profile in charging mode are presented in Fig. 9 and Fig. 10 while Fig. 11 and Fig. 12 illustrate them in discharge mode, respectively. According to the SOC profiles in Fig. 9 and Fig. 11, the equalization is achieved within a 1% SOC difference by all three methods. Besides,

TABLE I: PERFORMANCES COMPARISON FOR 8S4P CONFIGURATION

MODE	*Performance Index*	*Switch-based sequencing method [3, 4]*	*Dynamic resistance equalizer [5]*	*Proposed method*
CHARGE MODE	*DoSE (%)*	*98*	*98*	*98*
	Equ. Time (seconds)	*2000*	*3000*	*4200*
	$\sum P_{loss\_external}$ (W)	*0.28*	*1.37*	*0.51*
	$\sum P_{loss\_internal}$ (W)	*2.6*	*1.3*	*1.32*
	Total power loss (W)	*2.88*	*2.67*	*1.83*
DISCHARGE MODE	*DoSE (%)*	*98*	*98*	*98*
	Equ. Time (seconds)	*1600*	*2400*	*3200*
	$\sum P_{loss\_external}$ (W)	*0.64*	*2.56*	*1.03*
	$\sum P_{loss\_internal}$ (W)	*5.13*	*2.41*	*2.61*
	Total power loss (W)	*5.77*	*4.97*	*3.64*

battery modules can take a rest during phase B to help to prolong the lifetime of the battery.

The waveforms of the branch current and the module voltages in Fig. 13 describe the detailed operation of the proposed method in the discharging mode. As the voltage of module #4 is the lowest, the switching frequency of reactive balancing circuit for module #4 is set to 1kHz while the others are set to 10kHz. As a result, module #4 is discharged with the lowest current among them and the SOC is gradually equalized with each other. As the SOCs change, the role of the lowest module is dynamically assigned to the modules. When the SOCs of all modules become similar, the switching frequency of all reactive balancing circuit is set to 10kHz to minimize the power loss and distribute the current between branches evenly.

Based on the test results, the external and internal losses are calculated and summarized in Table I. The proposed method is found to be the most efficient method as the total power loss is the lowest among them. It is because the external loss of the proposed method is similar to the switch-based sequencing method while the internal loss is the lowest due to the switching pattern of current as in Fig. 13(a). The total loss of the proposed method is as small as 63.5% (in charging mode) and 63% (in discharging mode) of the total loss of the switch-based sequencing method.

4. CONCLUSION

This paper proposes a reactive balancing circuit for parallel-connected battery modules using dynamic capacitance modulation. In the idle mode, the SC cell exchanges charge between two modules one after another to gradually equalize SOCs of all modules. In the non-idle mode, it regulates the current distribution by modulating the equivalent resistance through frequency control. The HIL test results show that the equalization performance of the proposed method is superior to the conventional methods in view of the total power loss. The design optimization for the reactive balancing circuit shall be done and the hardware experiments will be prepared to further verify the performance of the proposed method.

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Energy Conversion
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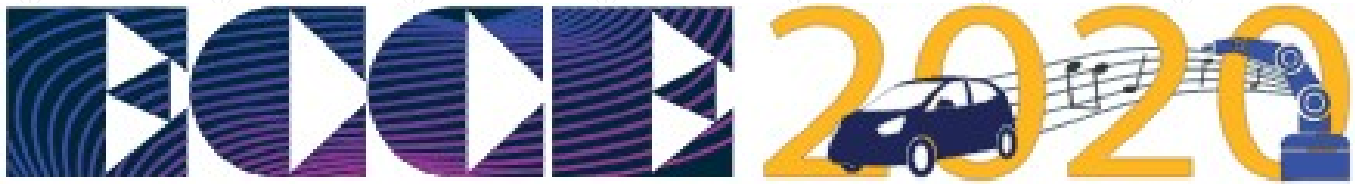

Reactive Balancing Circuit for Paralleled Battery Modules Employing Dynamic Capacitance Modulation

OCT. 12th, 2020

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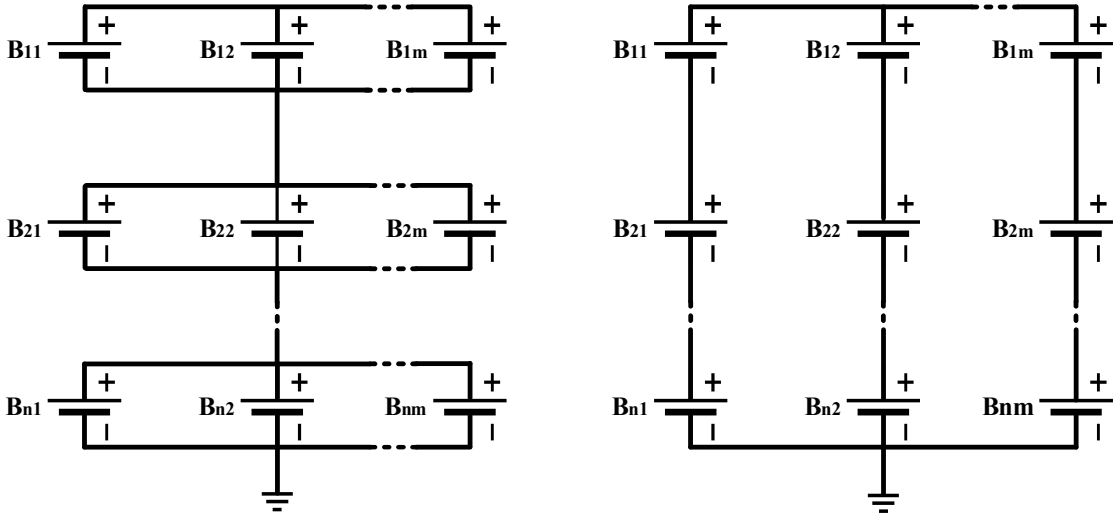
University of Ulsan, Republic of Korea

Contents

- *Introduction*
- *Conventional methods*
- *Proposed method*
- *Verifications*
- *Conclusion*

1. Introduction: Research motivation

- **Battery configuration in BESS and EV:**
  - Battery cells are connected in **series** to increase the **system voltage** and in **parallel** to enlarge the **system capacity**.
  - Two common configurations:
    - **mPnS**: ***m*** cells in **parallel** to form **a group**, ***n* groups** are connected in **series**.
    - **nSmP**: ***n*** cells in **series** to form **a module**, ***m* modules** are connected in **parallel**.

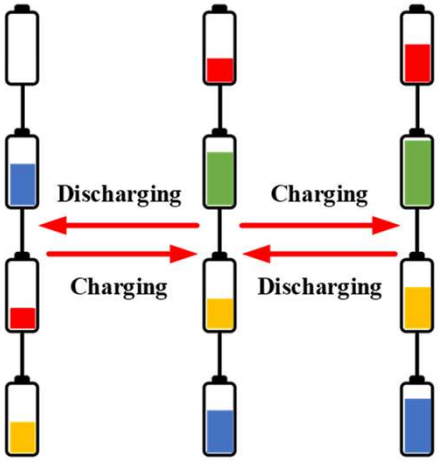


mPnS **nSmP**

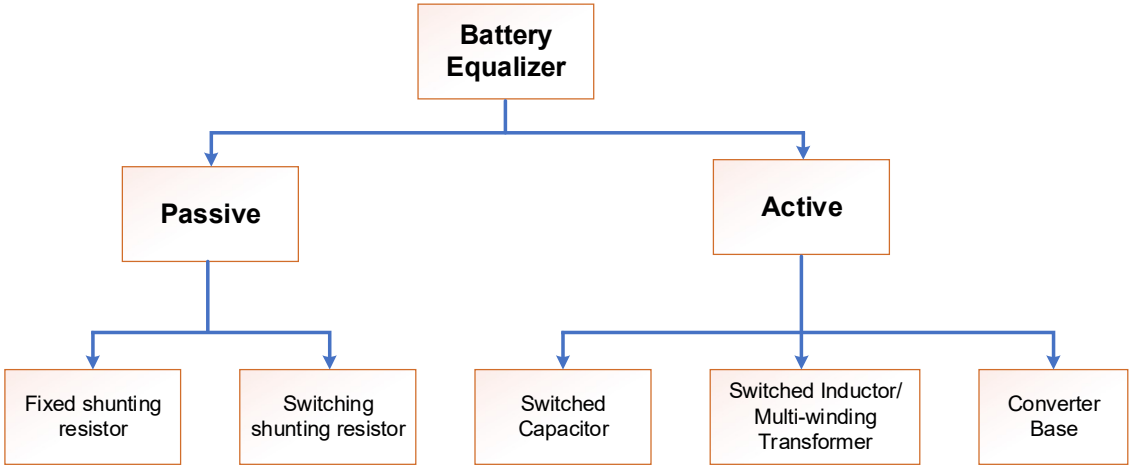
1. Introduction: Research motivation

- **Cell inconsistency in series battery connection**
  - The characteristics of battery cells are so different that it may causes:
    - Reduction of the available capacitance
    - Possible over-charging and over-discharging to the battery cells

  →Various battery equalizers have been published to solve this inconsistency issue.



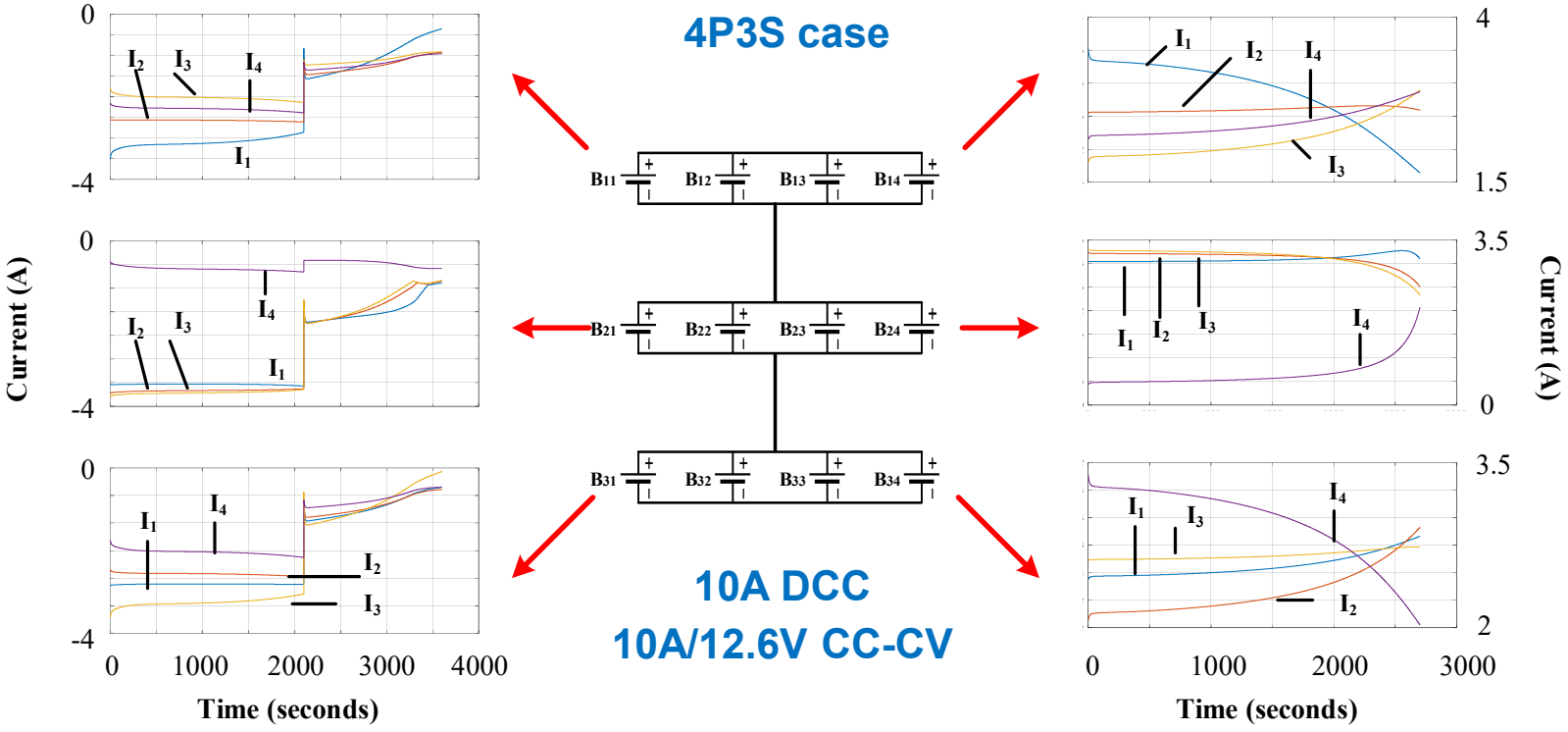
Unbalanced cells



Battery equalizer classification

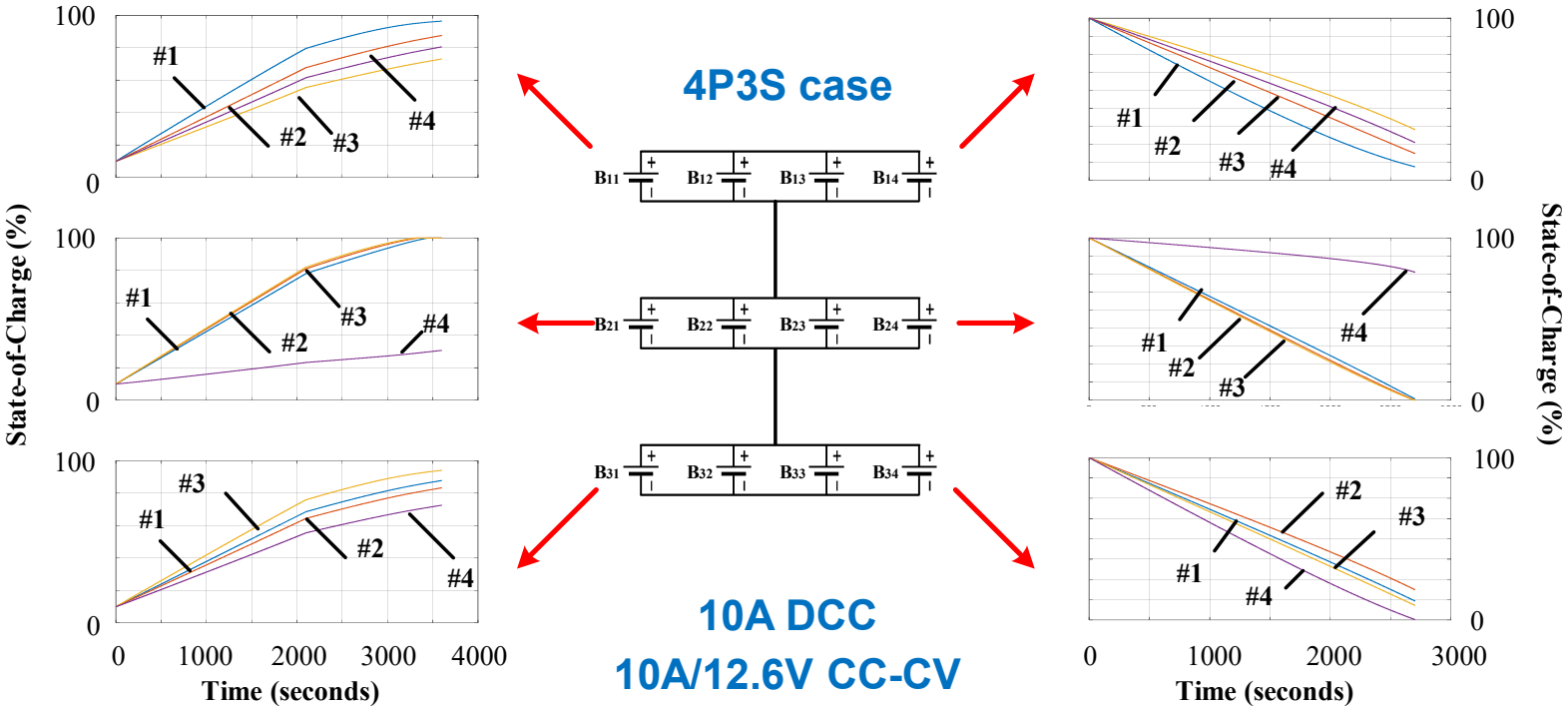
1. Introduction: Research motivation

- **Cell inconsistency in parallel battery connection** causes more serious problem than in the series configuration:
  - Unequal current sharing between branches in charging and discharging mode.



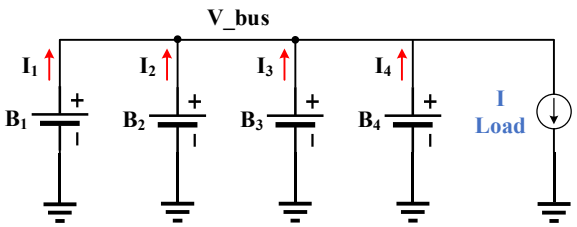
1. Introduction: Research motivation

- **The cells inconsistency in parallel batteries connection** causes the more serious problem than in the series configuration:
  - Reduction system capacity
  - Over-charge or over-discharge risks for the whole parallel connection

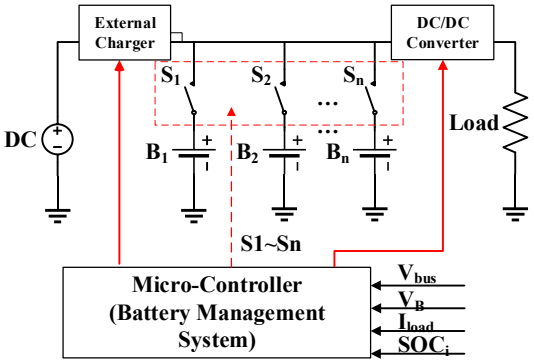


Charging mode **Discharging mode**

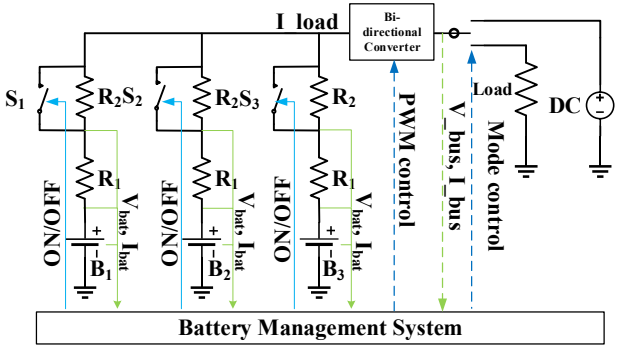
2. Conventional methods



Direct-connection



Switch-based sequencing [3, 4]



Dynamic resistance equalizer [5]

- **Conventional parallel-equalizer:**
  - **Direct-connection**: battery cell characteristics are **screened,** and the **similar cells** are **directly connected** together.
  - **Switch-based sequencing**: **one additional switch** is utilized, which is turned **on and off sequentially.**
  - **Dynamic resistance equalizer**: **two resistors and one switch** are utilized to regulate the branch current.

2. Conventional methods

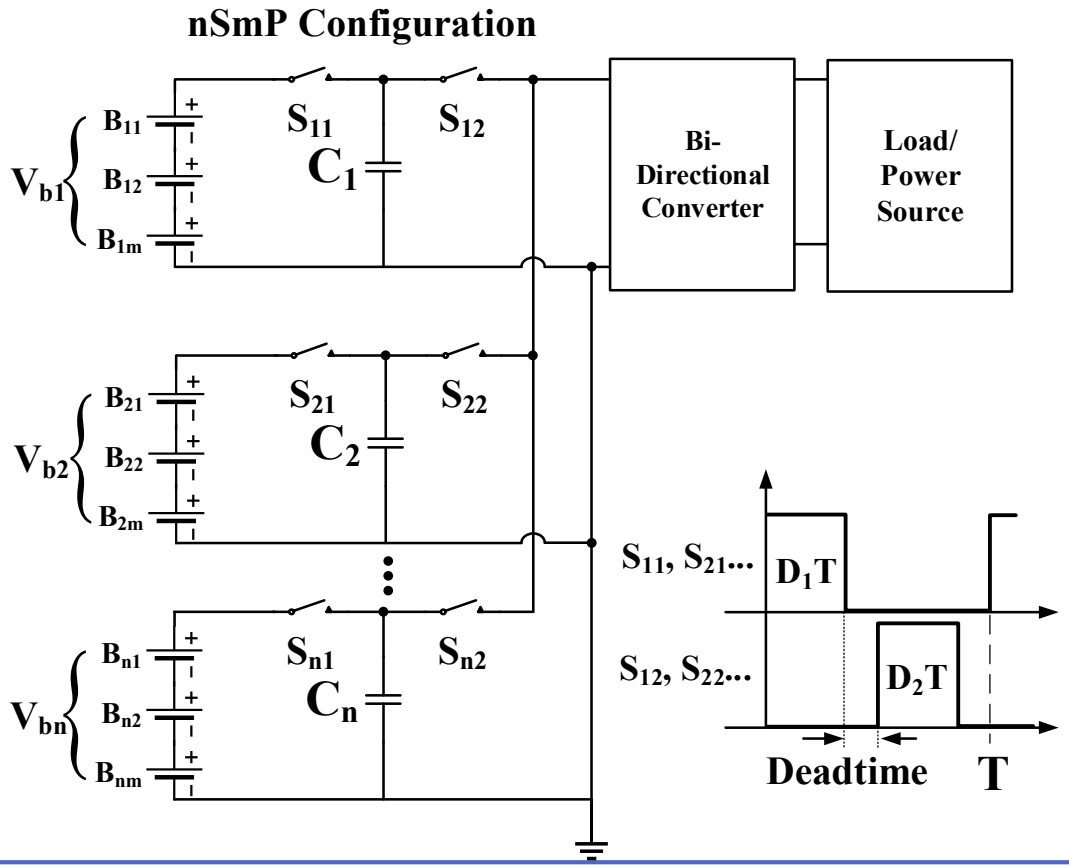
- **Fundamental problems of conventional parallel-equalizers:**
  - Because of **different aging patterns in battery cells**, the **reliability** of the direct-connection is **very poor.**
  - The switch-based sequencing method **balances the SOC** but the **unequal current sharing issue** is not yet resolved.
  - The dynamic resistance equalizer **balances the SOC and shares the current**, but the **power loss** is relatively high.
  - The equalization is achieved **only** when the system is working **in non-idle mode**.

➔A reactive equalizer for parallel battery modules, which has **high efficiency** and **good performance,** is required.

3. Proposed method

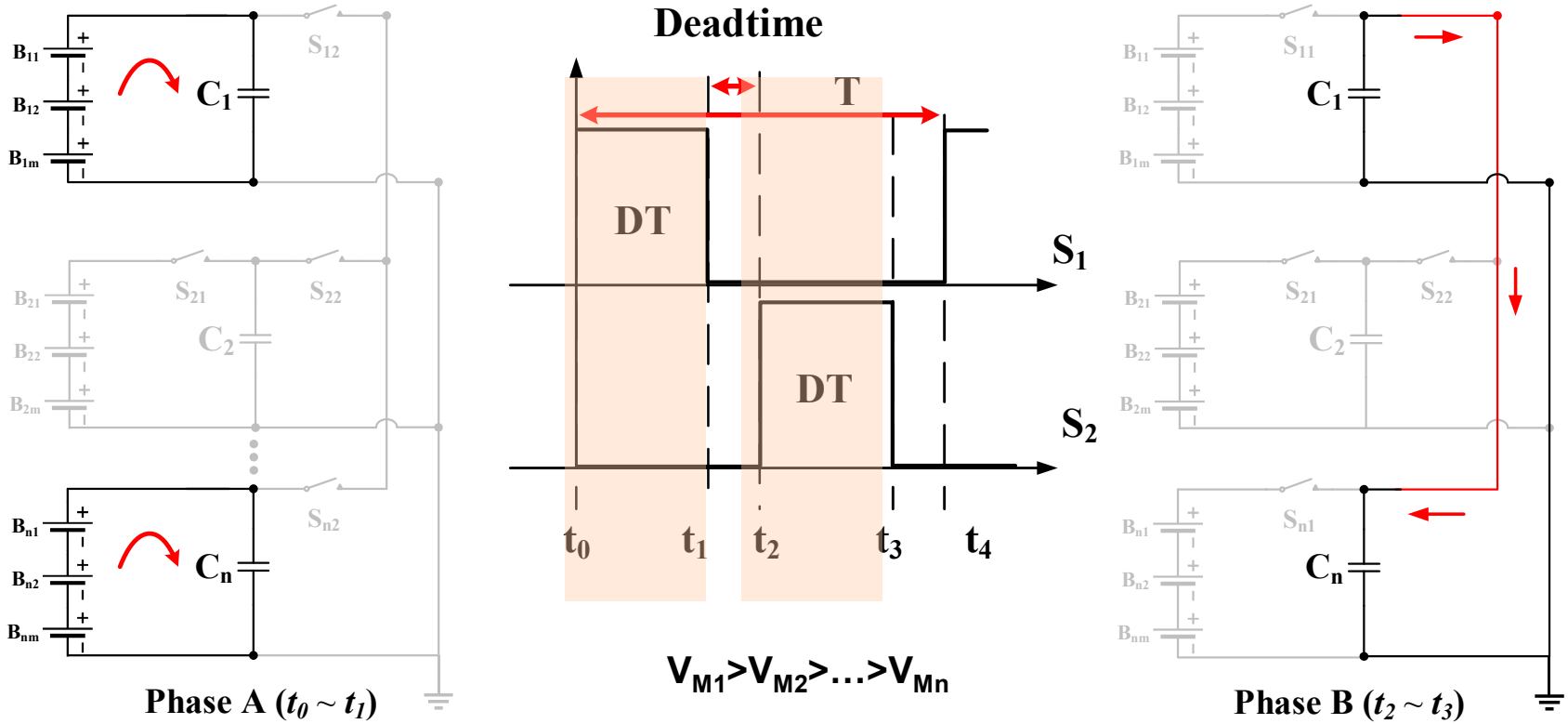
❑Circuit configuration:

- **Each battery module** connects to a switched-capacitor equalizer (**SC cell**).
- Outputs of SC cells are connected in **parallel**.



3. Proposed method

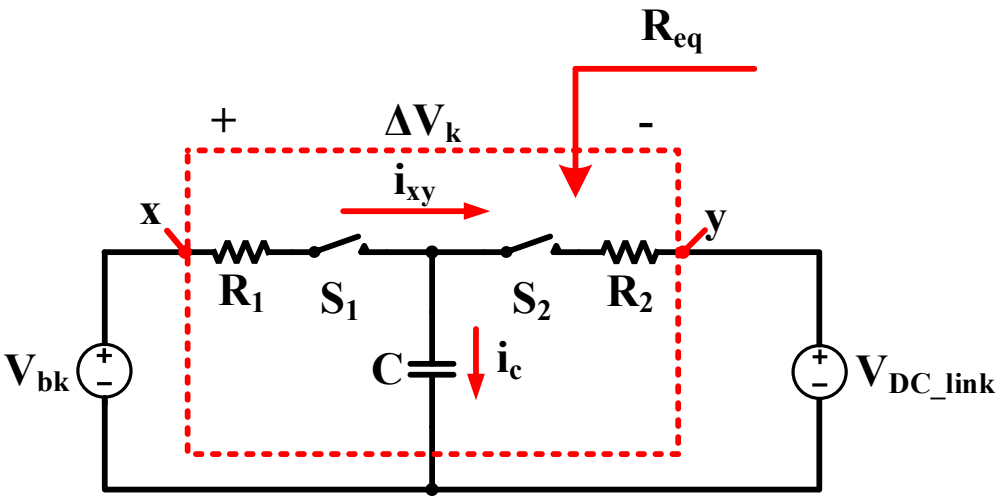
❑ Operating principle: Idle mode

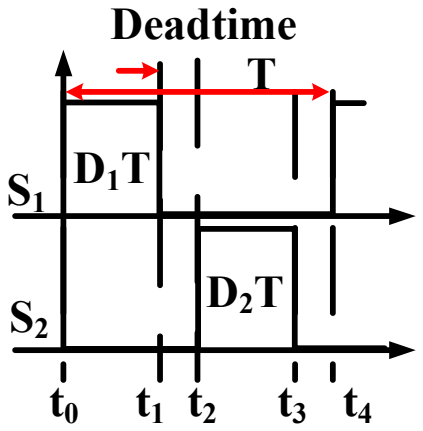


- **Voltages** of modules are **scanned**.
- The **left switches** of the **highest and lowest voltage** are turned ON.
- The **right switches** of the **highest and lowest voltage** are turned ON.

3. Proposed method

❑ Operating principle: non-idle mode





- In non-idle mode, the **SC cell** serves as a **variable resistance emulator**.
- The **equivalent resistance** of an **SC cell** is given by:

$$R_{eq} = \frac{1}{f_s C} \frac{exp(\frac{D_1}{f_s \tau_1}) exp(\frac{D_2}{f_s \tau_2}) - 1}{\left[exp(\frac{D_1}{f_s \tau_1}) - 1\right]\left[exp(\frac{D_2}{f_s \tau_2}) - 1\right]}$$

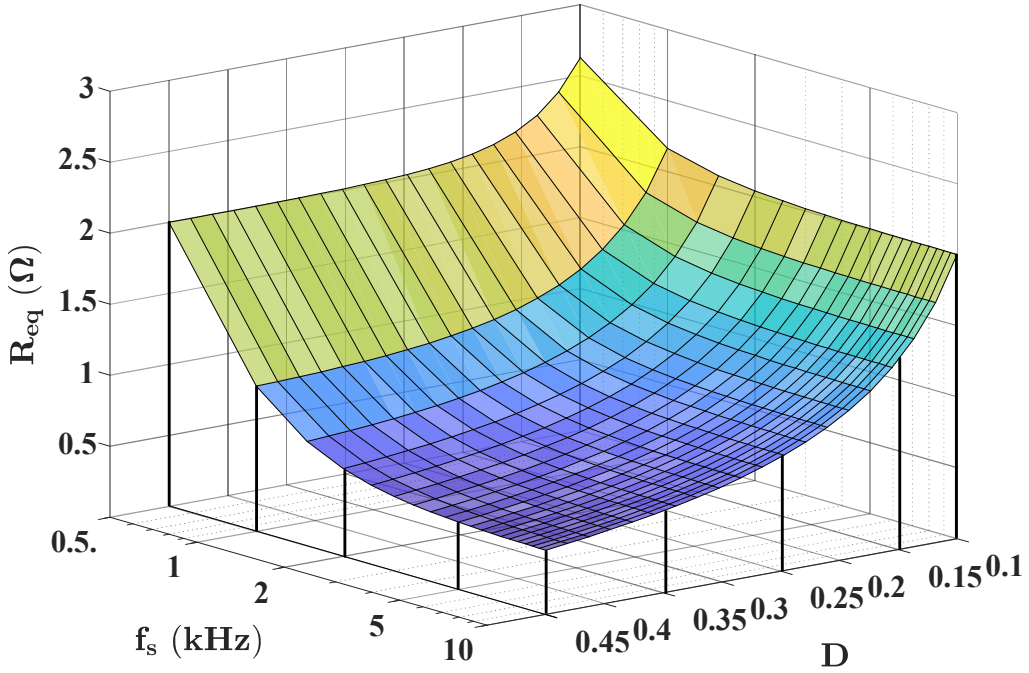
$$\tau_i = R_i C$$

$$R_i = R_b + R_{d,on} + ESR$$

$$i = 1, 2, \ldots, n$$

3. Proposed method

❑ *Operating principle: non-idle mode*



$$R_{eq} = \frac{1}{f_s C} \frac{1 + exp(\frac{-D}{f_s \tau})}{1 - exp(\frac{-D}{f_s \tau})}$$

$$C = 2200\mu F$$

$$R_i = 0.1\Omega \quad (i = 1, 2, \ldots, n)$$

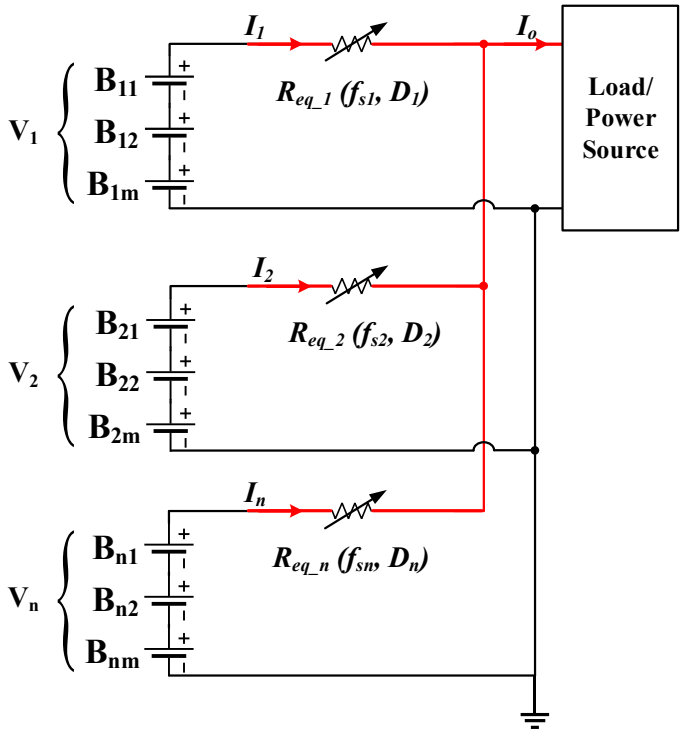
$$D_1 = D_2$$

$$\tau_1 = \tau_2$$

- The **equivalent resistance** can be regulated by **changing the switching frequency**, f_s, and the **duty cycle ratio**, D.
- The **switching frequency control** is adopted in this paper.

3. Proposed method

❑ Operating principle: non-idle mode



Current sharing equation:

$$I_1 R_{eq_1} - I_2 R_{eq_2} = V_1 - V_2$$

$$I_1 R_{eq_1} - I_3 R_{eq_3} = V_1 - V_3$$

$$\dots$$

$$I_1 R_{eq_1} - I_n R_{eq_n} = V_1 - V_n$$

$$I_1 + I_2 + \dots + I_n = I_o$$

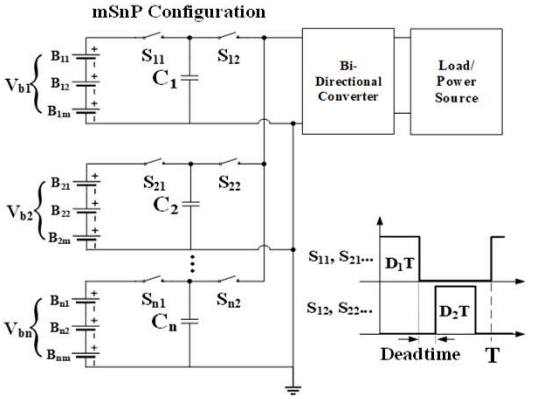
- The **load sharing** is achieved by the **difference between R_{eq}'s**.
- The SC cell for the **highest-voltage module** in case of **charging mode** or the **lowest-voltage module** in case of **discharging mode** is operating in a **lower switching frequency** to increase the equivalent resistance.

4. Verification: Test setup

- **Hardware-in-the-loop** tests are implemented for an **8S4P battery configuration** of 18650 Li-ion battery cells (3.6V – 2600mAh).
- The **equalization capacitance** of the SC cell is set to **2200uF**.

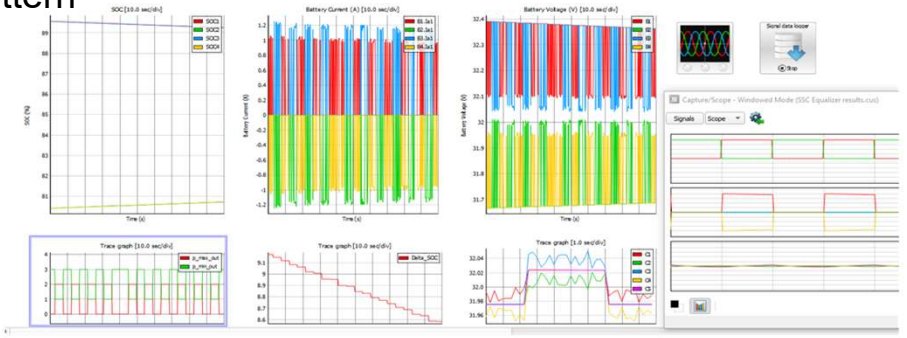
- Battery models
- SC cells
- Charging/discharging loads

Typhoon HIL 602+



Visualization

Control pattern



4. Verification: Test setup

- The **duty cycle** and **dead-time** are set to **45%** and **5%**, respectively.
- The switching frequency is controlled according to the operation modes.

	Idle	Charging	Discharging
Initial SOC	100, 80, 90, 70%.	15, **40**, 20, 30%.	100, 80, 90, **70**%.
Switching frequency	**10kHz**	**1kHz** for the **highest**-voltage module. **10kHz** for the **others**.	**1kHz** for the **lowest**-voltage module. **10kHz** for the **others**.

- External loss in the circuit is evaluated differently for three methods of balancing:

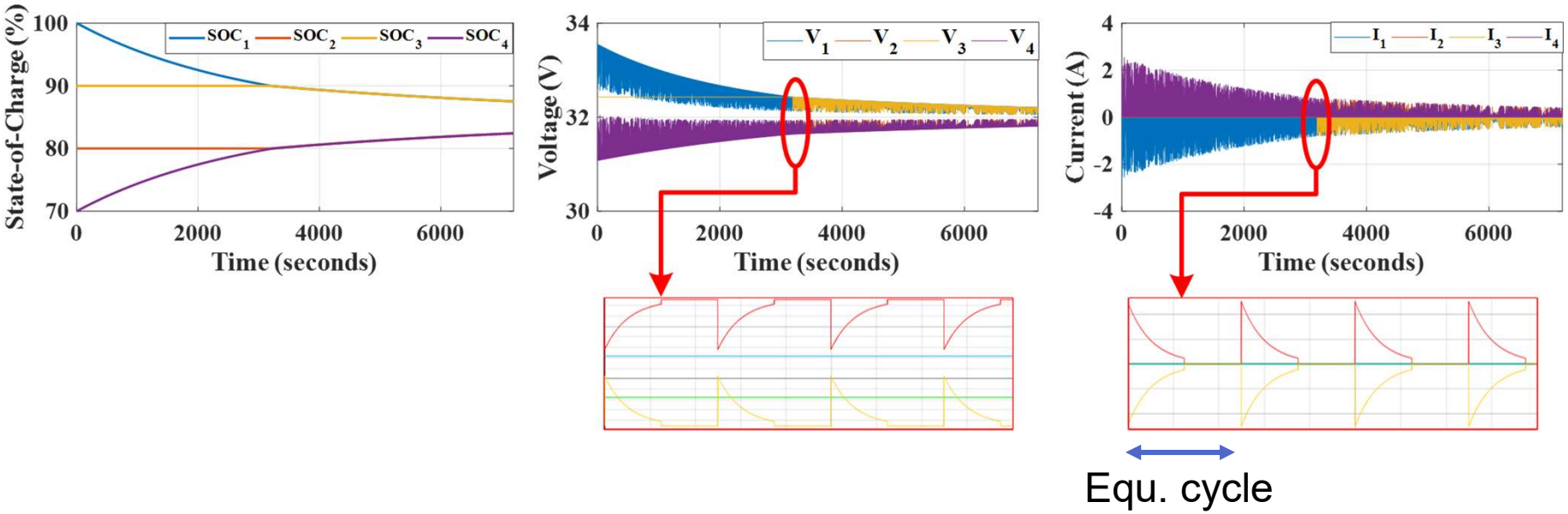
$$P_{external} = \sum_{m=1}^{N} \frac{1}{t_3} \int_0^{t3} i_m^2(t) Z_m(t) dt$$ **for proposed method, dynamic resistance equalizer**

$$P_{external} = \sum_{m=1}^{N} \frac{1}{t_3} \int_0^{t3} i_m^2(t) R_{d\_on} dt$$ **for switch-based sequencing method**

- Internal loss inside the battery cell is uniformly calculated by:

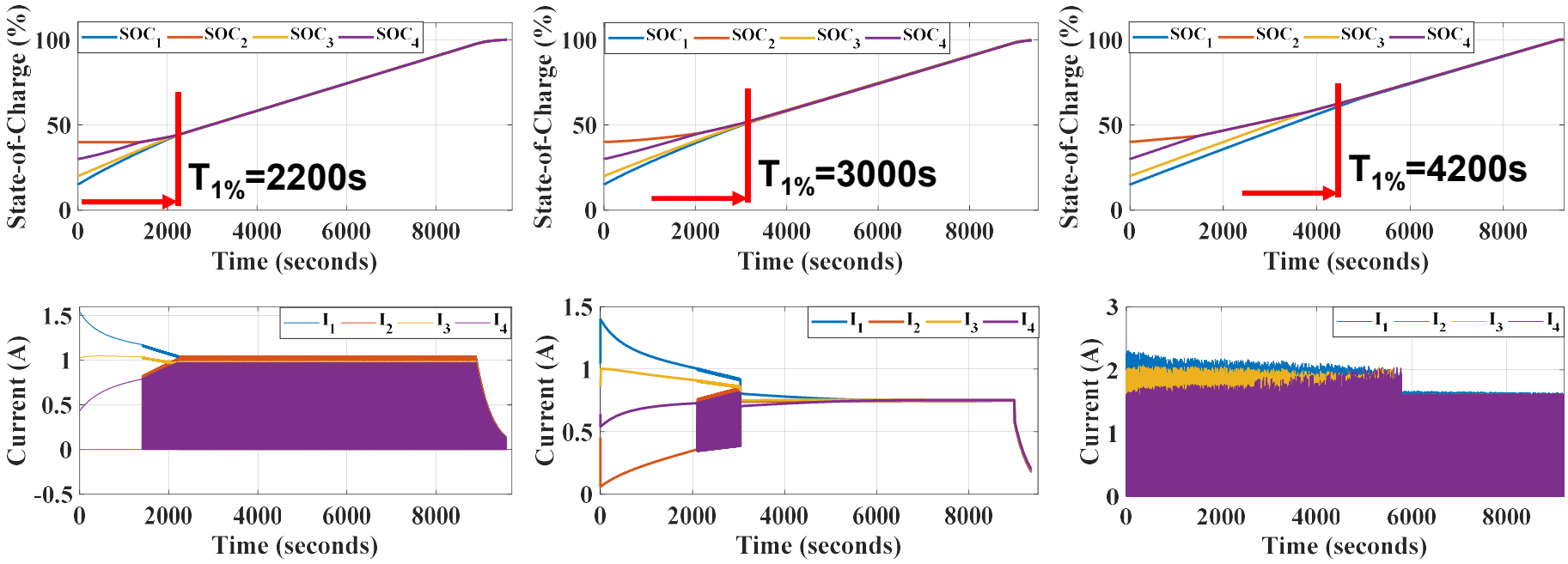
$$P_{internal} = \sum_{m=1}^{N} I_{rms\_m}^2 R_b$$

4. Verification: Idle mode of proposed method



- Only **two modules** are equalized in **one cycle**.
- The **SOC comparison algorithm** dynamically change the **switching pattern** during the equalization process.
- The **SOC and voltage differences** are equalized within **5% and 0.4V** at the end of the process.

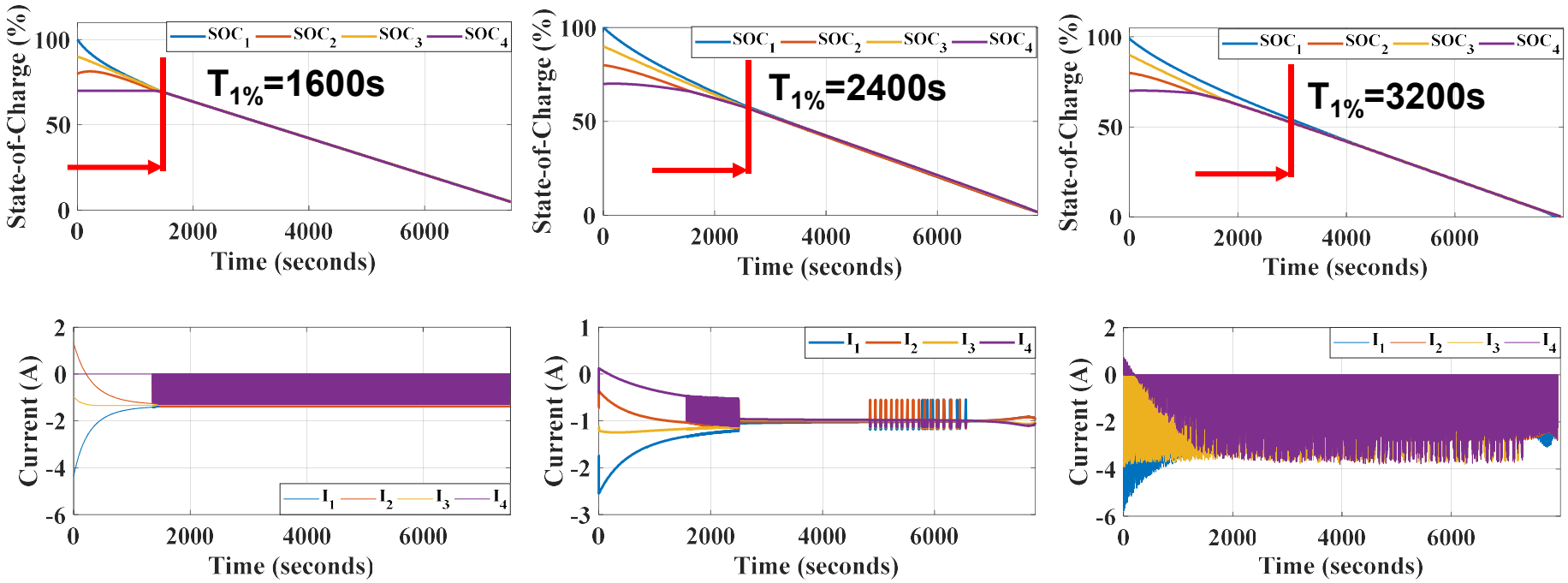
4. Verification: Charging mode



Switch-based sequencing | **Dynamic resistance equalizer** | **Proposed method**

- The **SOCs of all modules** are equalized **within 1%** and fully charged in the end.
- Proposed method requires about **4200 seconds** to achieve **1% SOC difference equalization**.

4. Verification: Discharging mode



Switch-based sequencing | Dynamic resistance equalizer | Proposed method

- The **SOCs of all modules** are equalized **within 1%** and fully discharged.
- Proposed method requires about **3200 seconds** to achieve the **1% SOC difference equalization**.

4. Verification: Performance comparison

Mode	Performance Index	Switch-based Sequencing	Dynamic Resistance Equalizer	Proposed Method
Charging Mode	DoSE (%)	98	98	98
	$T_{1\%}$(s)	2200	3000	4200
	$\sum P_{loss\_external}$ (W)	0.28	1.37	0.51
	$\sum P_{loss\_internal}$ (W)	2.6	1.3	1.32
	Total loss (W)	2.88	2.67	**1.83**
Discharging Mode	DoSE (%)	98	98	98
	$T_{1\%}$(s)	1600	2400	3200
	$\sum P_{loss\_external}$ (W)	0.64	2.56	1.03
	$\sum P_{loss\_internal}$ (W)	5.13	2.41	2.61
	Total loss (W)	5.77	4.97	**3.64**

*__DoSE__: Degree of SOC Equalization after balancing process:

$$DoSE = \frac{\Delta SOC_{initial} - \Delta SOC_{final}}{\Delta SOC_{initial}}$$

5. Conclusions

- **This paper proposes a reactive equalizer for parallel battery modules.**
  - The switched-capacitor cells serve as the **charge exchanger in case of idle mode** and **variable resistance** in case of non-idle mode.
    - The energy is transferred from **any-module to any-module directly** in idle mode.
    - The branch-currents are **regulated by the switching frequency control** to balance the SOCs during the **non-idle mode**.
- **The proposed method generates a lower total power loss than conventional methods.**
  - In idle mode, the **SOCs and module voltages** are respectively equalized **within 5% and 0.4V** in the end of the equalization process.
  - In non-idle mode, the **power loss** of the proposed method is about **63%** of the **switch-based sequencing**.
  - Because the proposed method presents a **slower balancing speed** than other methods, a **trade-off study** will be carried on to find the **optimal operation strategy**.

THANK YOU FOR YOUR ATTENTION

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